Project ANR INSCOOP

Task 4: SUBSTRATE PATTERNING AND SITE CONTROLLED CATALYST ON SOI WAVEGUIDE

T4.1 : Catalyst patterning on Si (or STO/Si) and on SiO_2 /Si (or SiO_2 / STO/Si) (LTM-INL)

T4.1.1 Catalyst patterning on full sheet Si (or STO/Si) substrates (LTM)

T4.1.2 Catalyst patterning on SiO_2 /Si (or SiO_2 /STO/Si) (INL + LTM)

T4.2: Catalyst patterning on SOI waveguides (CEA, LTM)

T4.2.1 SOI waveguides (CEA)

T4.2.2 Catalyst patterning on SOI waveguides (CEA + LTM)

Bassem Salem-LTM
Pedro Rojo-Romeo-INL
Jean-Marc Fedeli / Badhise Ben Bakir-CEA-Leti

Deliverables of T4

D4.1 : PtIn and In catalysts patterning on silicon substrates **M12 (M0 to M12)**
D4.2 : PtIn and In catalysts patterning on nanoholes-SiO2/Si(001) **M12 (M6 to M12)**
D4.3 : PtIn and In catalysts patterning on STO/Si(001) **M24 (M12 to M24)**
D4.4 : Waveguides on SOI **M12 (M6 to M12)**
D4.5 : Catalyst patterning on SOI waveguide **M18 (M12 to M18)**

Potential blocking points and associated milestones

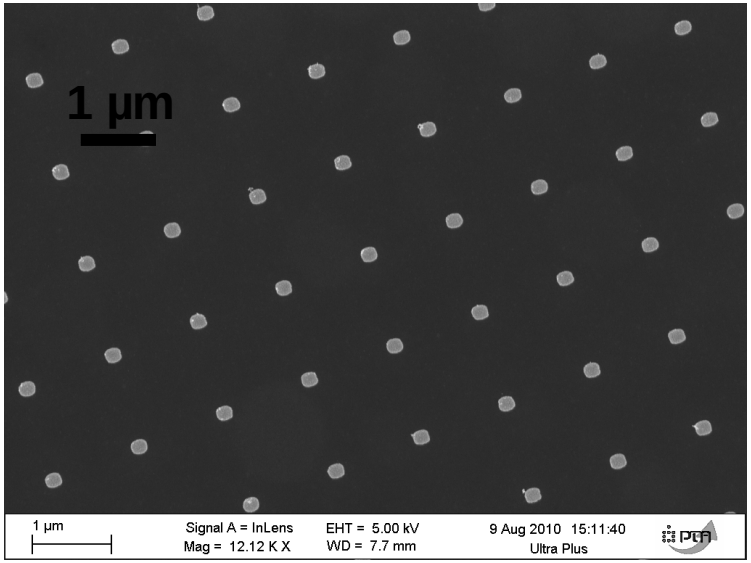
- Problem of STO etching?
- Growth on patterned substrate : InP deposition at the edge of the waveguide

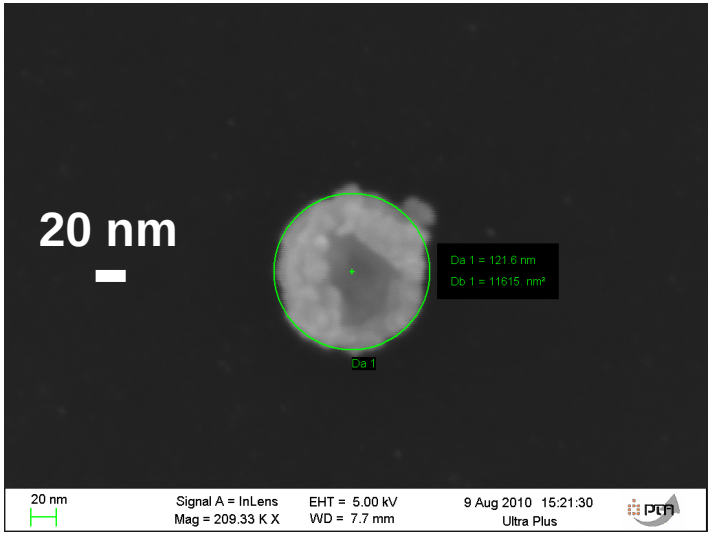
Milestones :

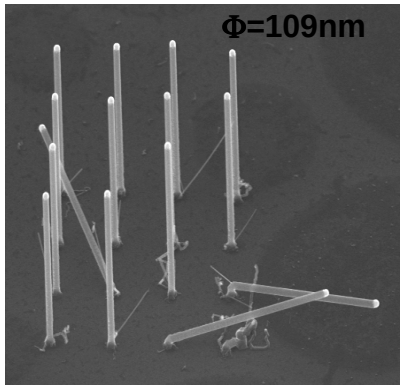
Do we add an additional technological step to remove InP from the edges of the waveguide?

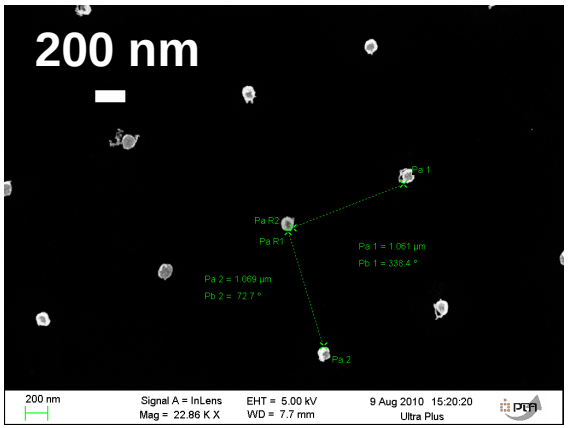
Savoir faire LTM: localisation des catalyseurs

Localisation des catalyseurs par e-beam : diamètre 50-300 nm

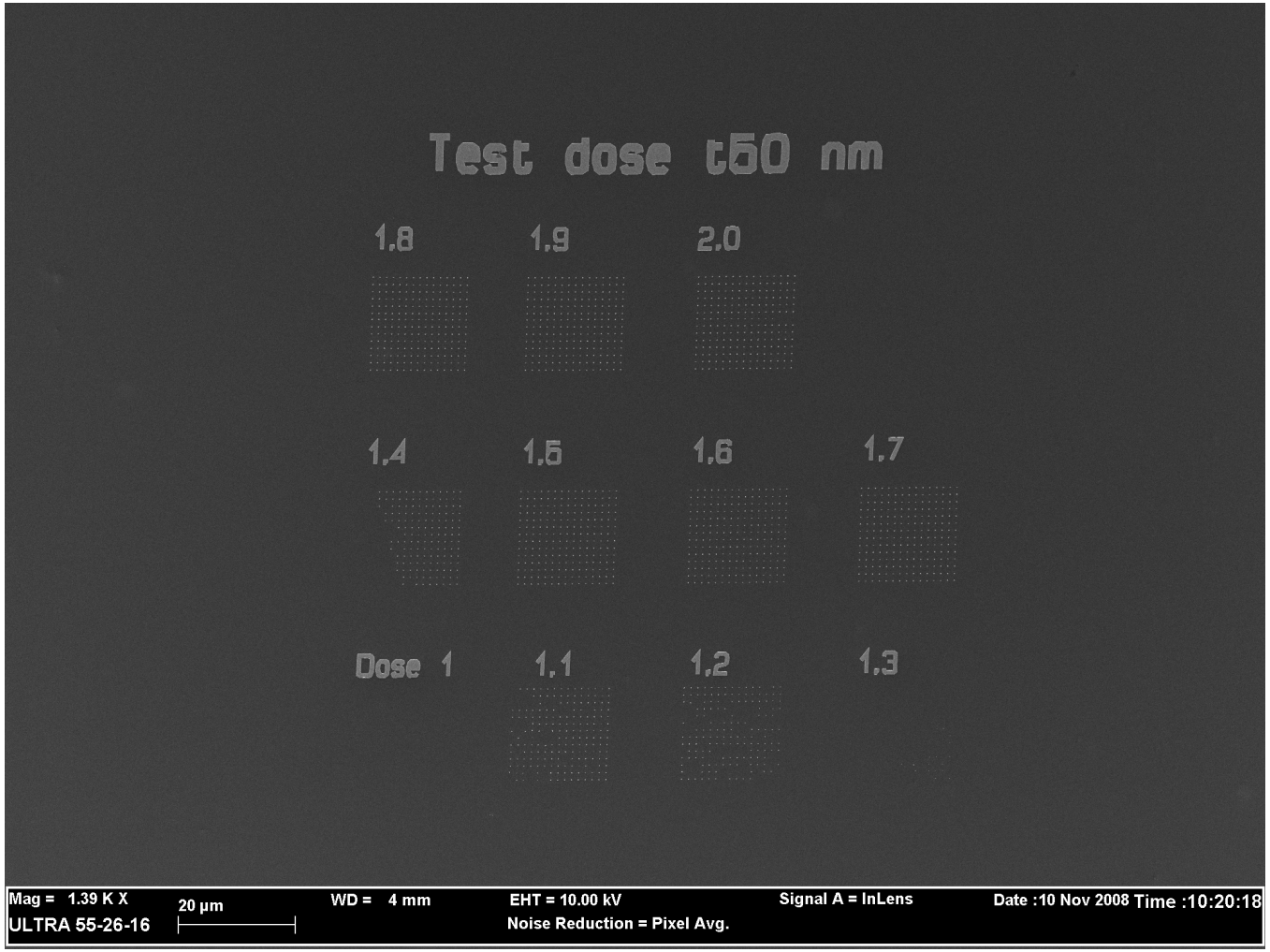




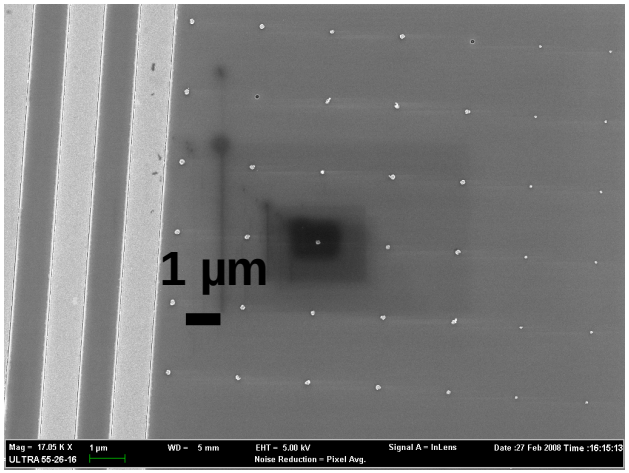


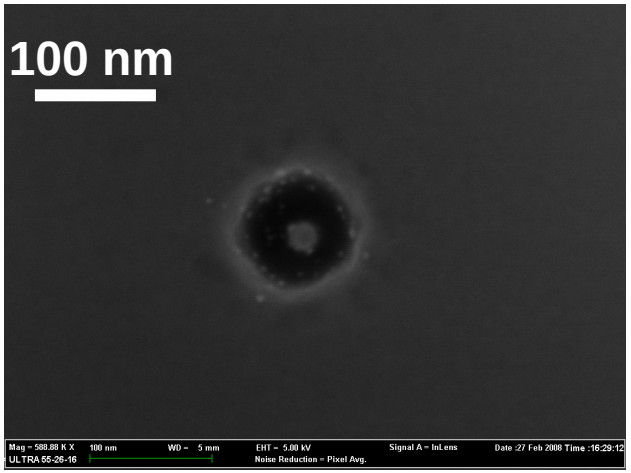


Localisation de plots d’Au (EBL-PTA)

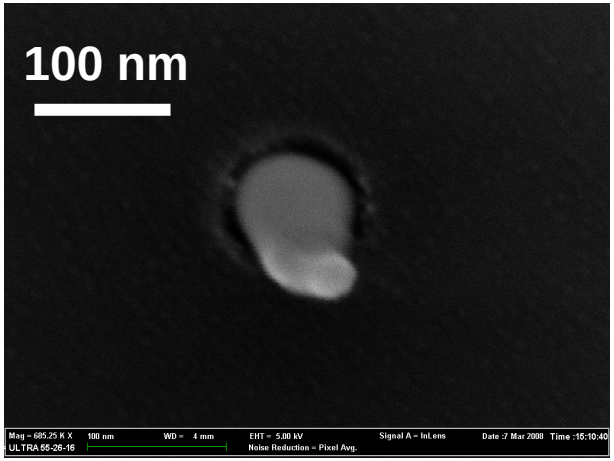


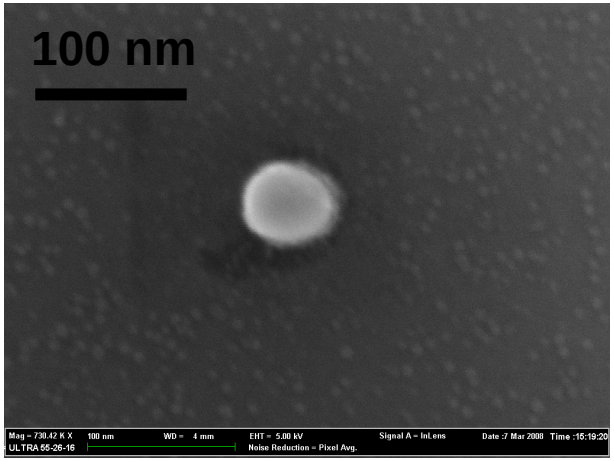
Localisation des catalyseurs dans une cavité (SiO_2) « masquer PTA »





Dépôt d'Au+lift-off



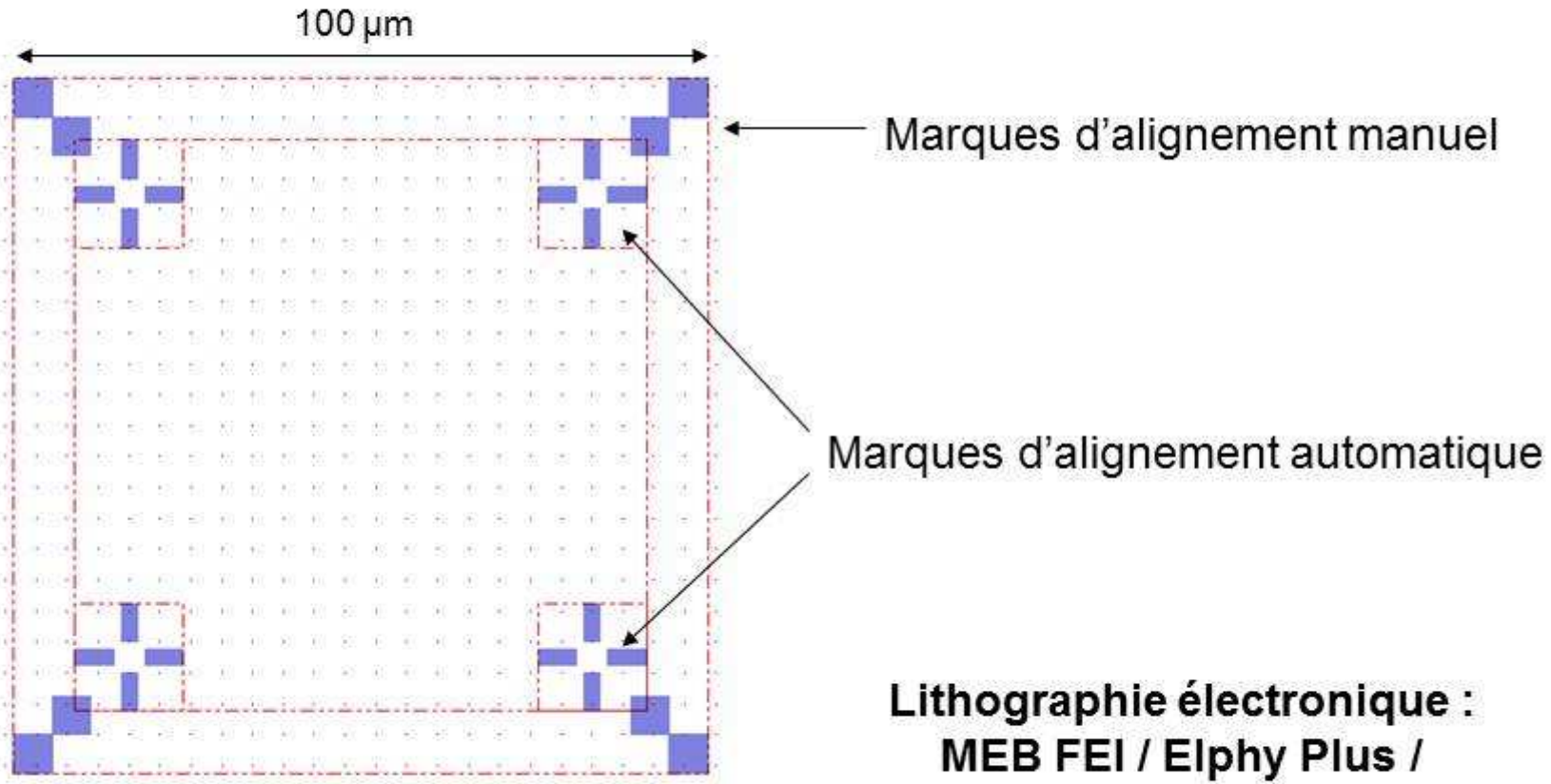


Croissance de nanofils

Savoir faire de l’INL

Croissance de nanofils contrôlée spatialement

Marques en lithographie optique



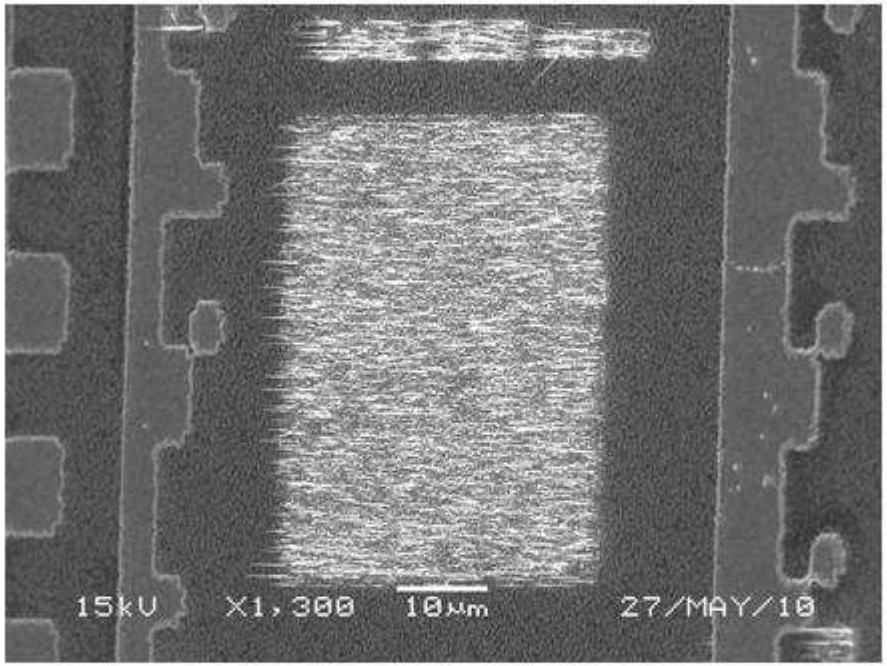
Lithographie électronique :
MEB FEI / Elphy Plus /
platine alignement laser

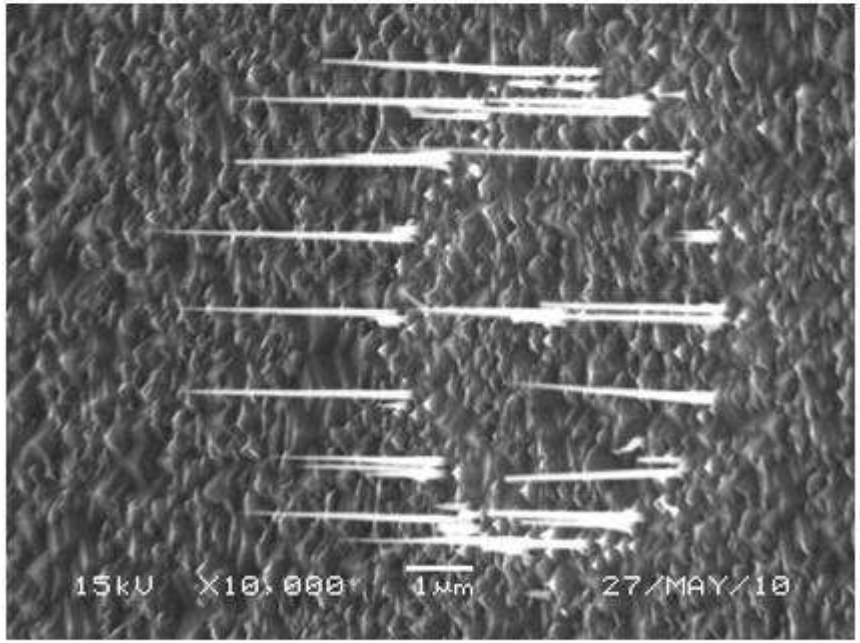
Résultats passés (InP et Si)

InP

InP <111>

Surface pleine
50µm x 50µm



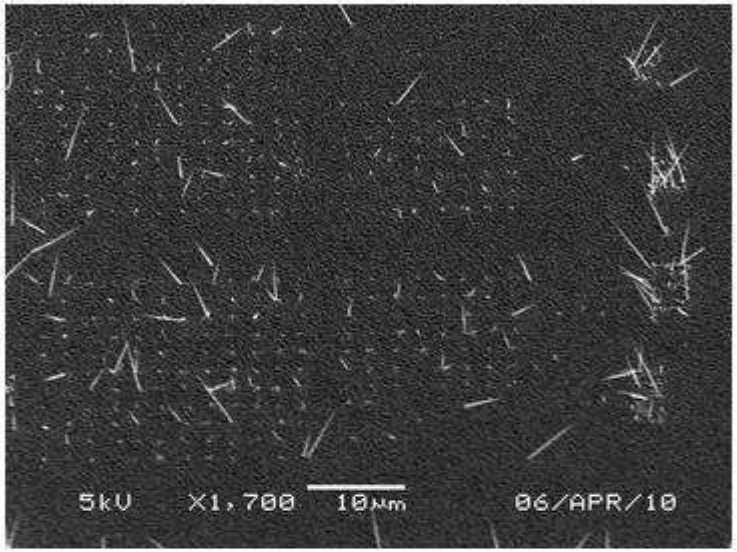


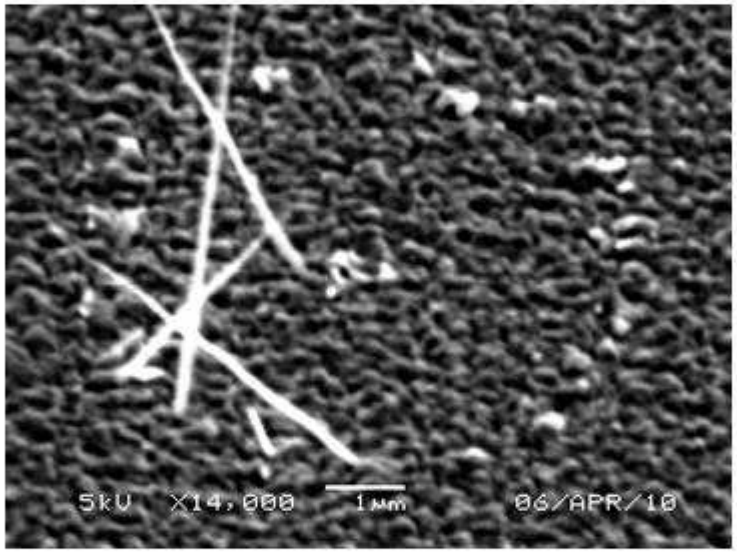
Sur plots Au localisés
(lithographie électronique)

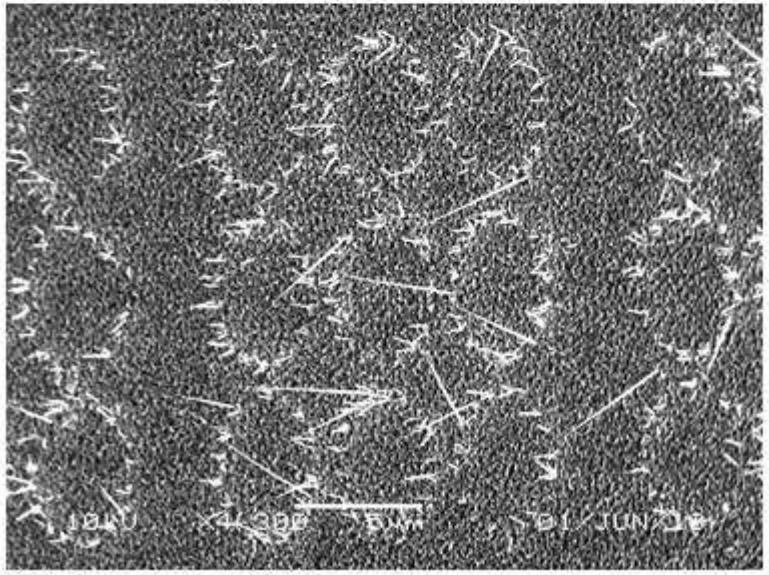
Résultats passés (InP et Si)

Si

Si <111>
Plots In/Au







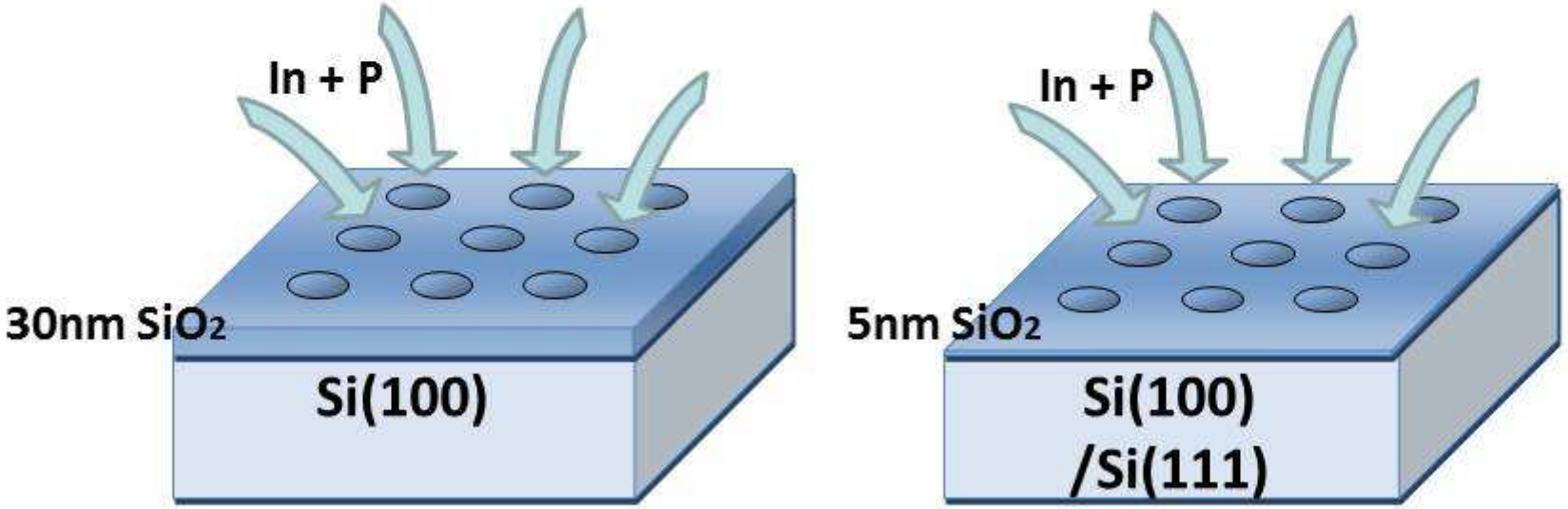
Problème de la taille des plots de catalyseur

Croissance sélective sur masque de silice

(Stage M1 Cao Ruping)

- Croissance sélective de nanofils InP sur substrat Si masqué
- Masquage par lithographie électronique et gravure
- Avec et sans catalyseur

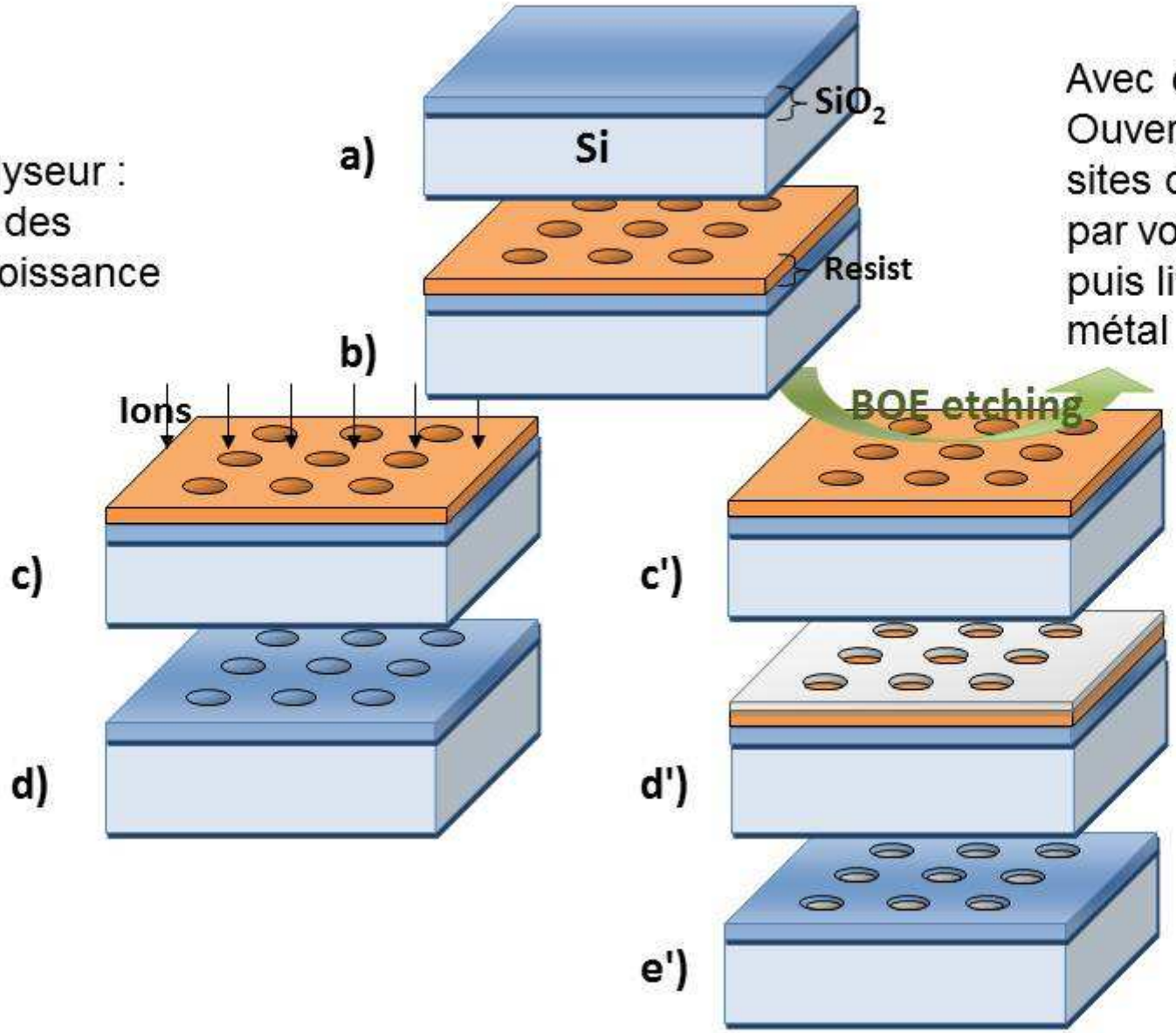
Substrats étudiés



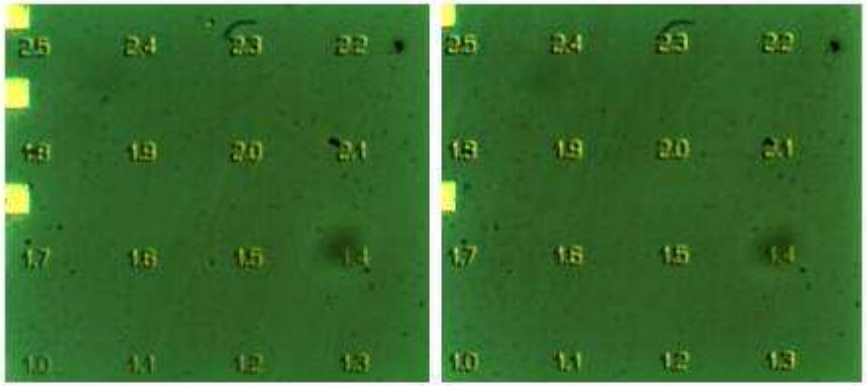
Process

Sans catalyseur :
Ouverture des sites de croissance par RIE

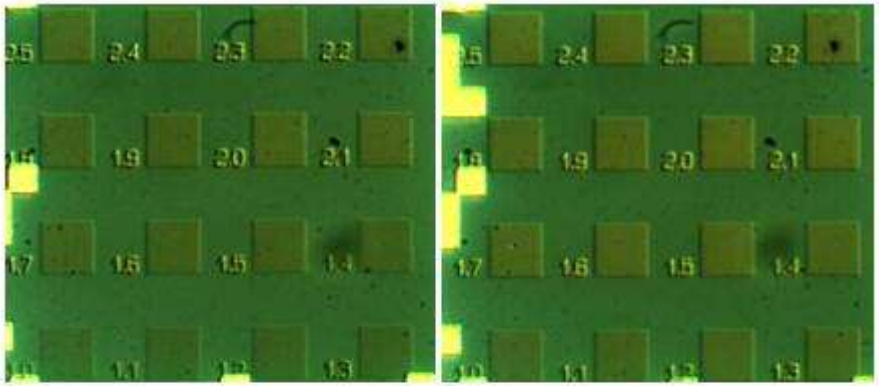
Avec catalyseur :
Ouverture des sites de croissance par voie chimique, puis lift-off de métal



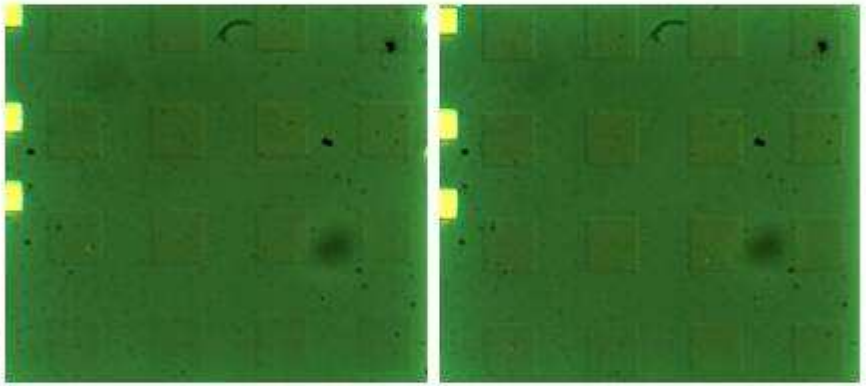
Réseaux de trous de 50 nm à 300 nm



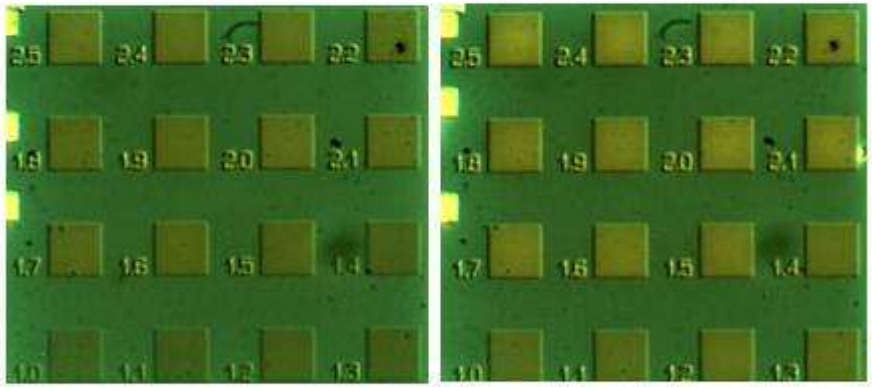
a)
50nm array



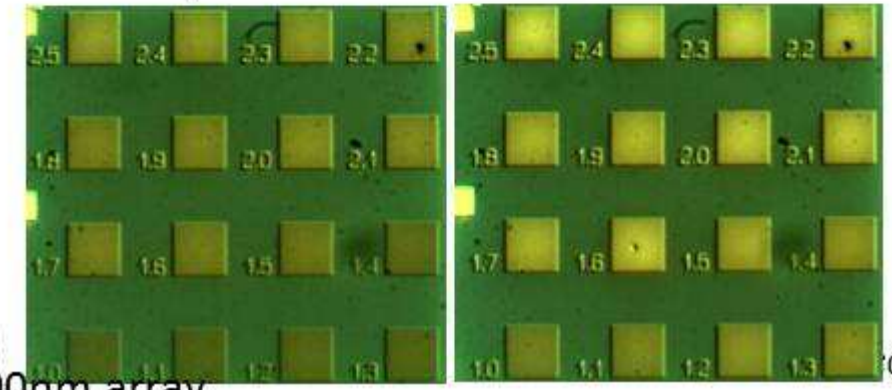
c)
200nm array



b)
100nm array



d)
250nm array

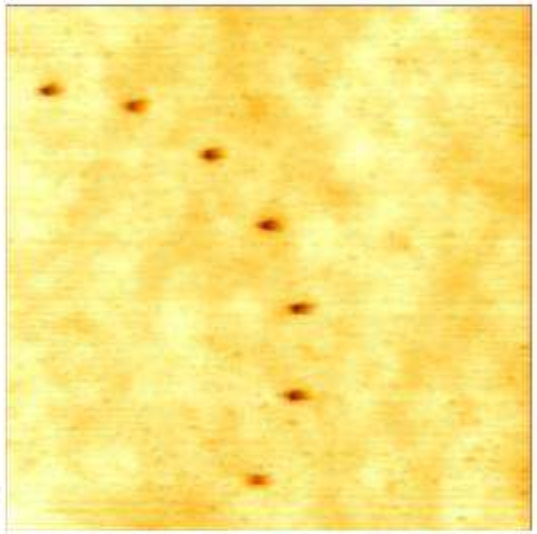


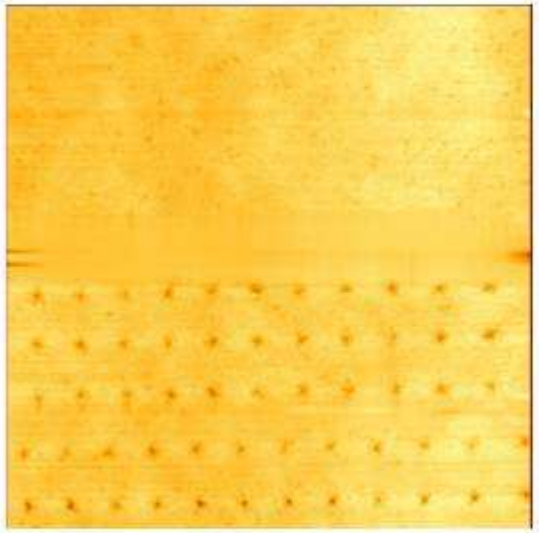
e)
300nm array

Problème : ouverture résine et silice pour les plus petits diamètres (50nm) non résolue

AFM

Si <100> 30nm SiO2 (PMMA monocouche, gravure Silice RIE 3').

a) 

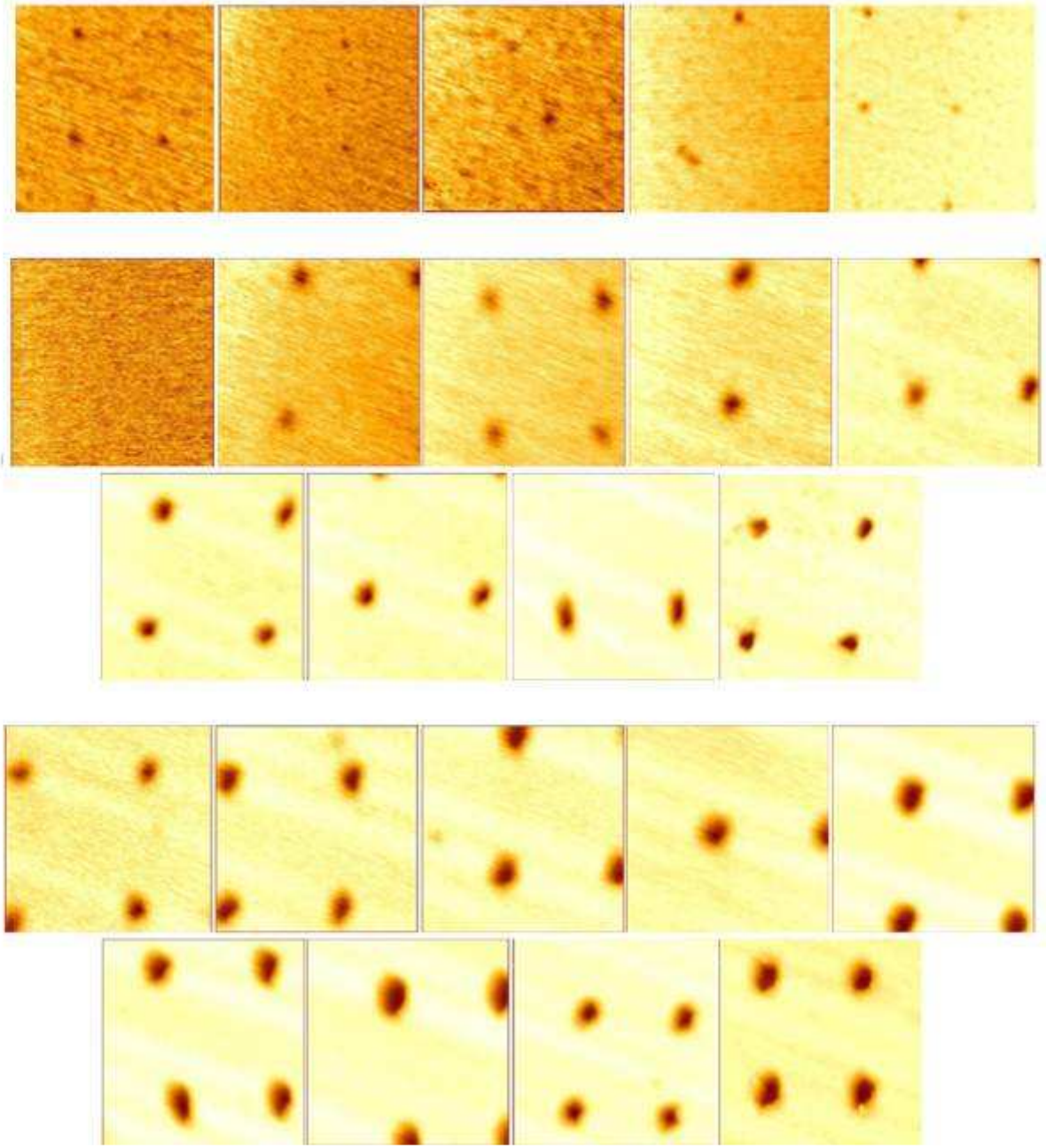
b) 

- AFM (1µm × 1µm) sur Si <100> 30nm SiO2 (PMMA monocouche gravure RIE 10').

a)
50nm array

b)
100nm array

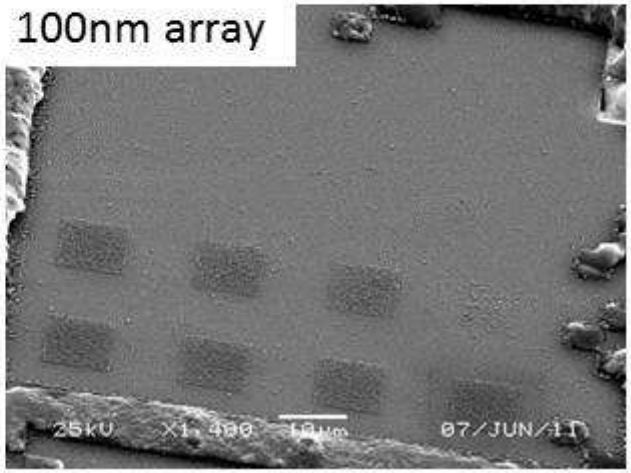
c)
150nm array



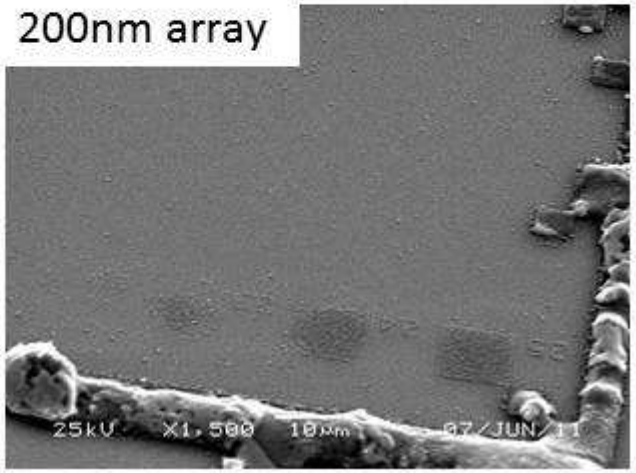
Croissance MBE (premiers essais)

Si <100> 30nm SiO2,
RIE 5'.
Épitaxie :
In (1") / In + P (10"),
450°C.
Rapport V/III : 10

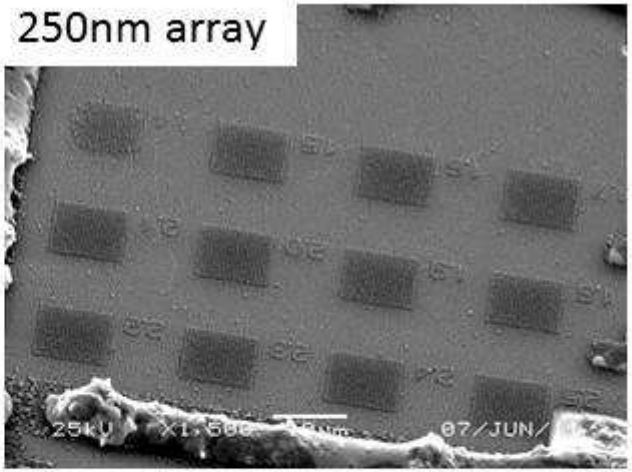
c)



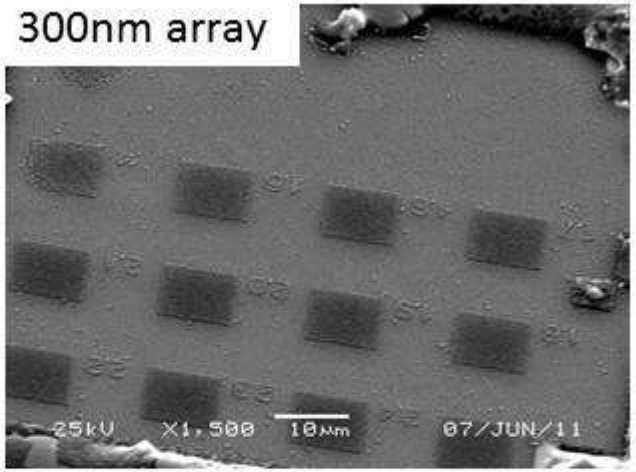
d)

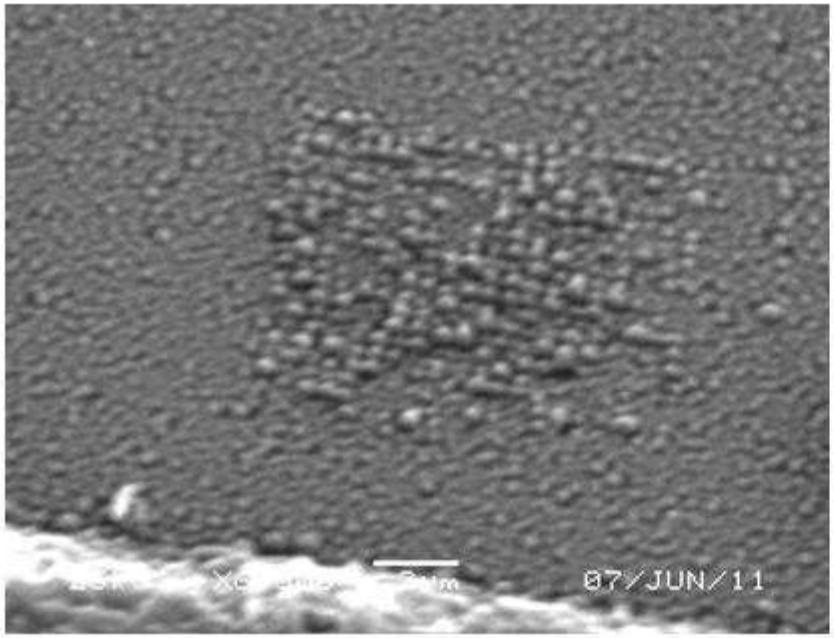


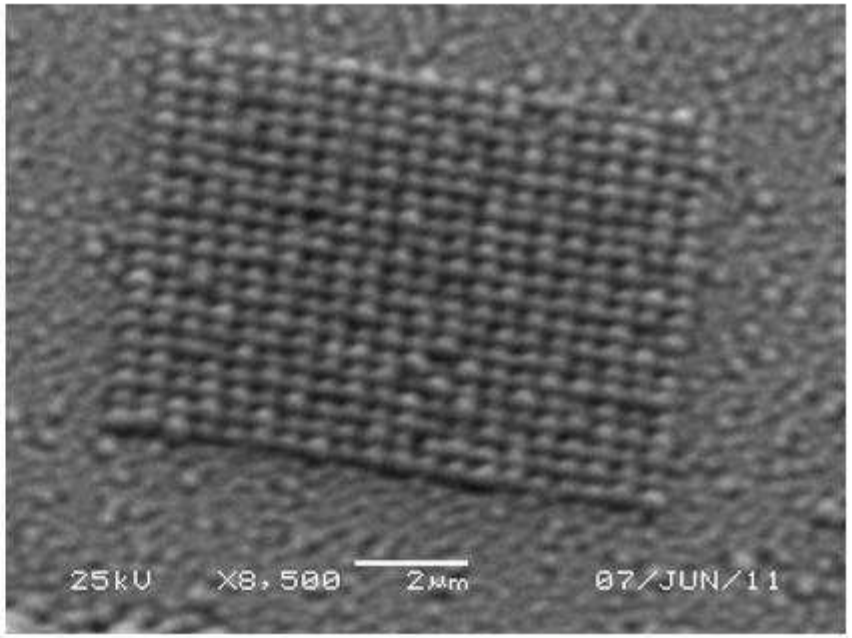
e)



f)



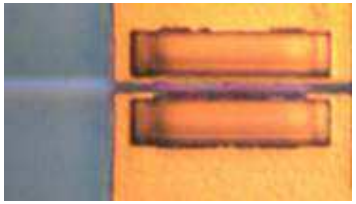


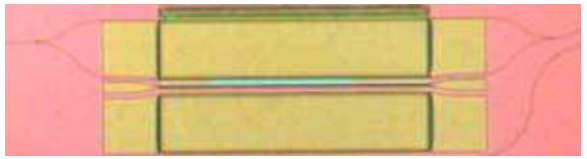


- caractérisation des profils des sites de croissance difficile
  - RIE (profondeur suffisante) / BOE (élargissement des trous)

- Localisation de la croissance d'InP, mais pas de nanofils
  - conditions de lithographie / dépôt à optimiser
  - conditions de croissance à optimiser

Photonic integrated circuits @CEA-Leti

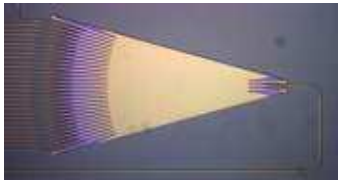


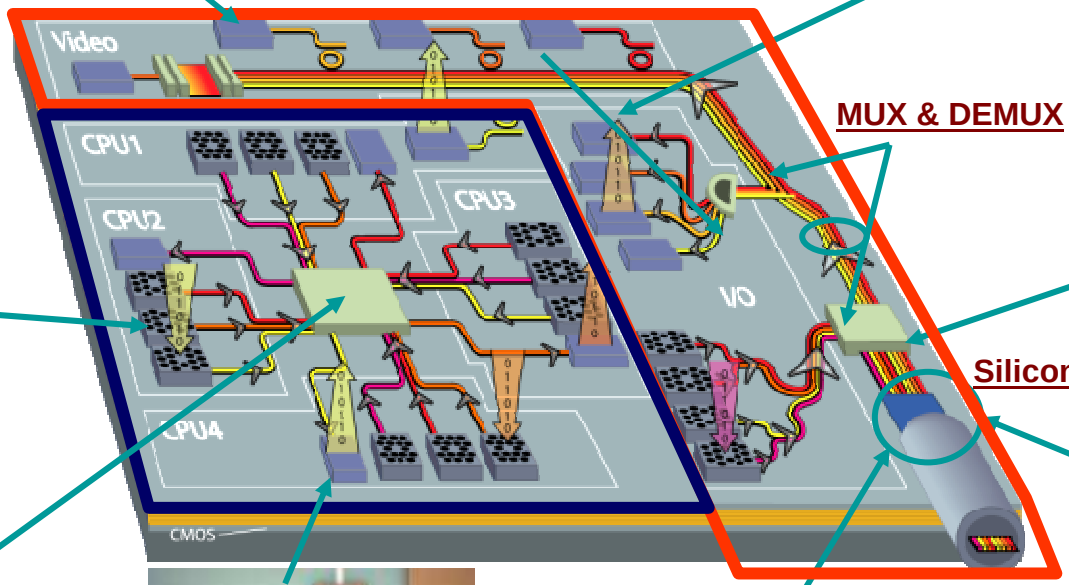


Ge-on-Si integrated photodetector

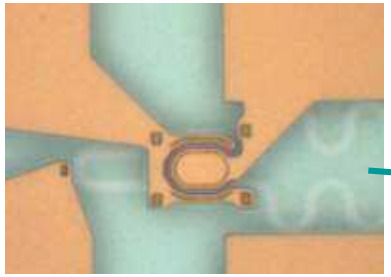
InP-on-Si integrated laser

Silicon optical modulator





MUX & DEMUX

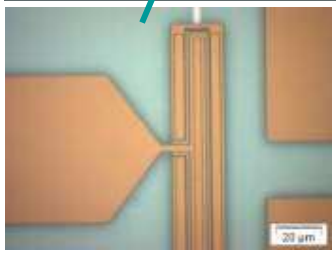


InP-on-Si integrated µlaser

Silicon-On-Insulator waveguide

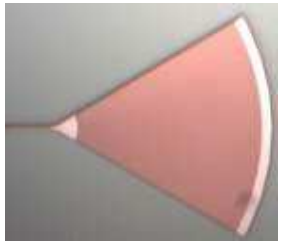
Grating coupler

Optical switch



InGaAs-on-Si integrated photodetector

Inverted taper



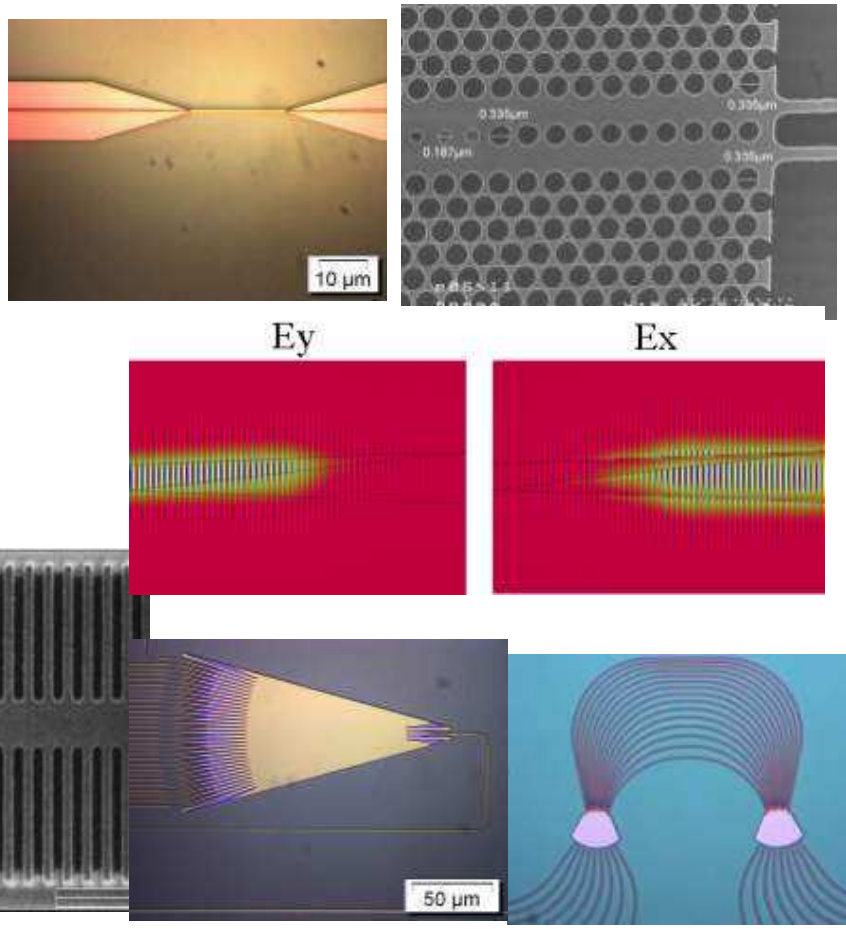
T4.2.1 SOI waveguide (CEA)

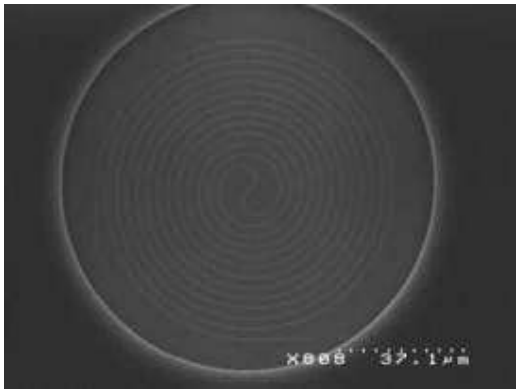
- CEA will contribute towards the design and realization of the passive waveguides. It includes:
  - the SOI waveguides (Strip or rib configuration),
  - tapering section between the NW area and the waveguide
  - as well as coupling structures (grating couplers or inverted tapers) to couple the light off the chip.

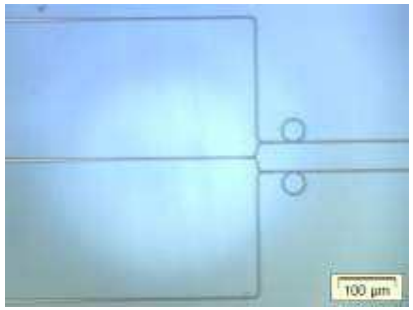
This task will be made in close collaboration with the tasks T5.1 to optimize the design of SOI waveguides. The passive waveguides will then be fabricated on 200 mm SOI wafers using 193 nm DUV lithography.

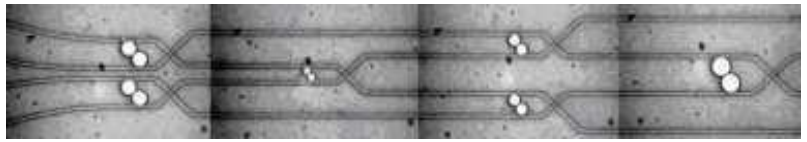
Passive silicon circuitry

- Waveguides
- Adiabatic transitions
- Splitters (wavelength, polarization)
- Polarization rotator
- MMI
- Resonators
- AWG (MUX, DMUX)
- oNoC (lambda-router)
- Slow wave structure, etc…



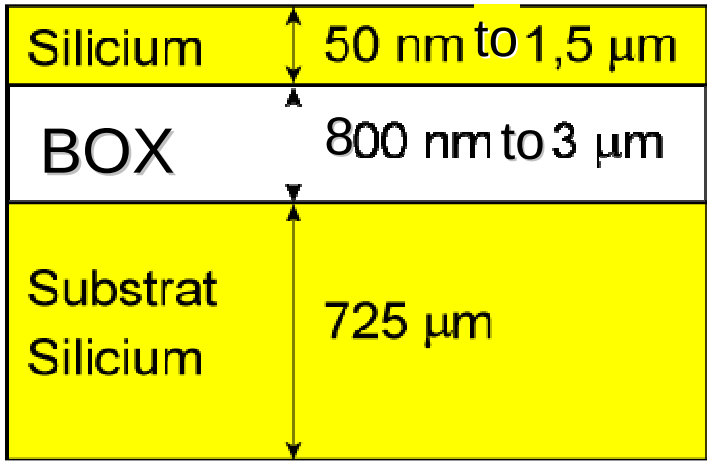


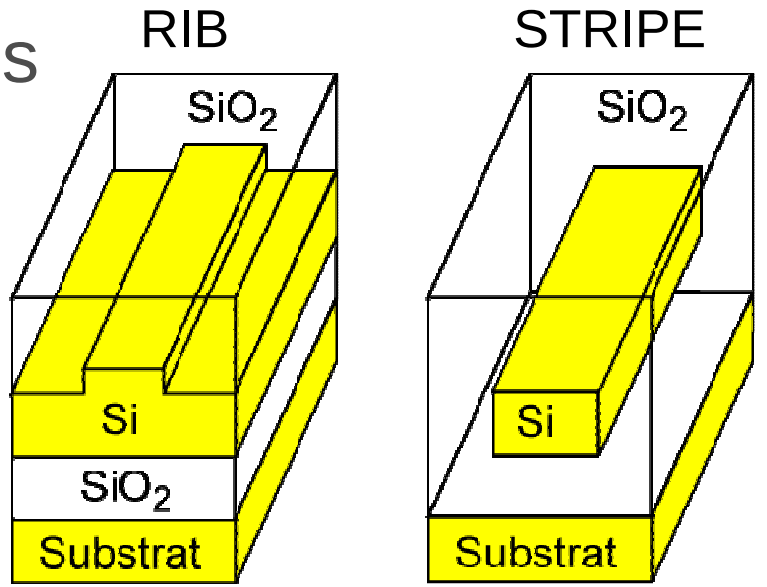




Si waveguide

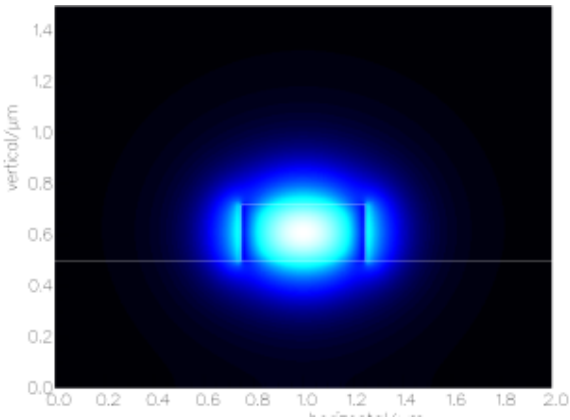
Silicon optical waveguides





Propagation losses:

- Strip waveguide <3dB/cm
- Rib waveguide <1dB/cm

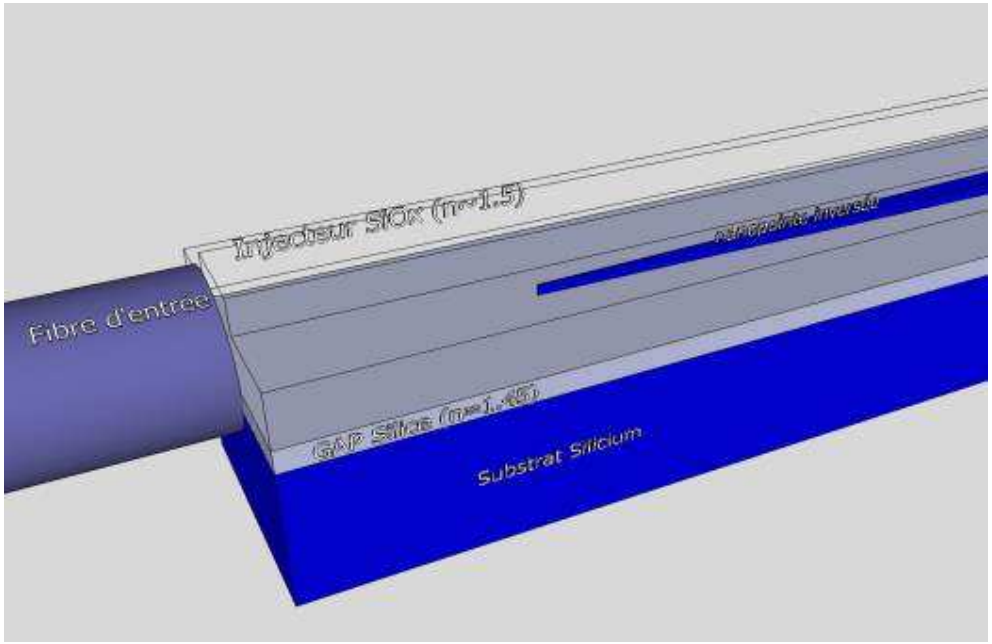


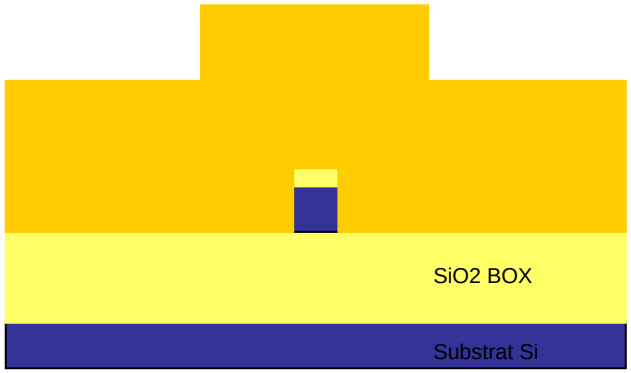
High refractive index difference with SiO_2

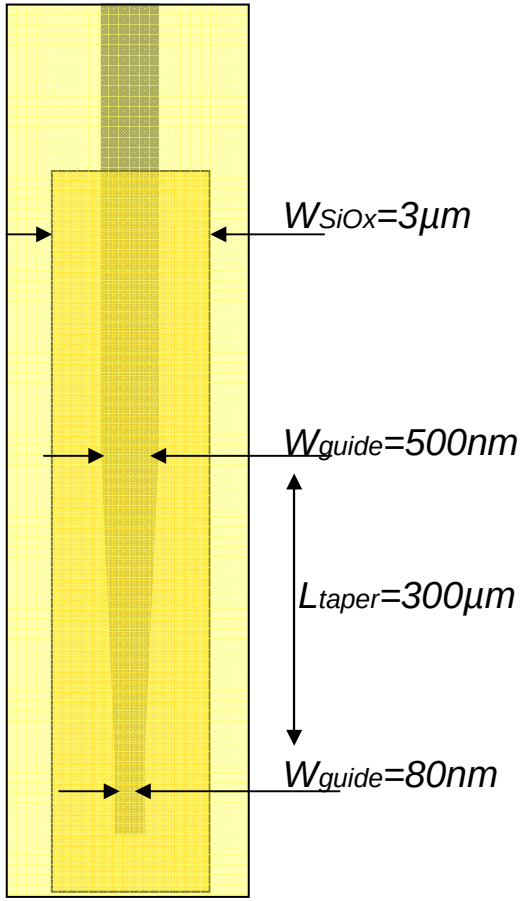
n_{Si}=3.5

n_{SiO2}=1.45

Edge fiber coupler







Edge fiber coupler